CHENG LIU

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Institute of Computing Technology, Chinese Academy of Sciences

No.6 Kexueyuan South Road, Haidian, Beijing, China

BIOGRAPHICAL SKETCH

Dr. Liu is an Associate Professor at the State Key Laboratory of Processors (SKLP), Institute of Computing Technology (ICT), Chinese Academy of Sciences (CAS). He received his Ph.D. from The University of Hong Kong in 2016, and his Master' s and Bachelor' s degrees from Harbin Institute of Technology in 2009 and 2007, respectively.

Dr. Liu's research interests focus on domain-specific architectures, with an emphasis on deep learning accelerators, coarse-grained reconfigurable architectures, graph processing accelerators, and FPGA-based accelerators. His work integrates hardware/software co-optimization to achieve design goals such as energy efficiency, performance, and reliability. He has authored over 70 publications in leading international conferences and journals. Among his awards are the Best Paper Award at the Great Lakes Symposium on VLSI (2021) and IEEE Transactions on Computers (2021), as well as the CAS Outstanding Award for Technological Achievements Transformation (2019) and the Huawei Olympus Award (2024). His research group has achieved top placements in international competitions, including the CVPR Low-Power Computer Vision Challenge, the DAC System Design Competition, and the ICCAD EDA Competition.

Dr. Liu serves as an Associate Editor for IEEE Transactions on Emerging Topics in Computing and as a Technical Program Committee (TPC) member for major conferences including DAC, FPT, ICLR, and AAAI. He is also a reviewer for leading IEEE journals such as TCAD, TVLSI, TPDS, TC, TECS, and TRETS. He is a senior member of IEEE and CCF, and a member of ACM.

EDUCATION & APPOINTMENTS

Associate Professor, Institute of Computing Technology	*2018-06 - now*
Research Fellow, National University of Singapore	*2016-12 - 2018-06*
Ph.D. Computer Engineering, The University of Hong Kong	*2011-09 - 2016-11*
M.E. Electronic Engineering, Harbin Institute of Technology	*2007-09 - 2009-07*
B.E. Electronic Engineering, Harbin Institute of Technology	*2003-09 - 2007-07*

ACADEMIC SERVICE

2024-now: Associate Editor of IEEE TETC

2022: TPC of DFT, FPT, CFTC

2023: TPC of ATS, FPT, DFTS, CFTC, NeurIPS

2023: Registration Chair of ATS

2024: TPC of DFTS, FPT, ICLR, ICML

2025: TPC of FPT, DFTS, DAC, AAAI, ICLR

2018-now: Reviewer for TCAD, TVLSI, TC, TPDS, TECS, TRETS, and others

RESEARCH GRANTS

[PI] Cross-Layer Processor Optimization Infrastructures, CAS, 11,000,000¥	*2024 - 2028*
[PI] Reliability Evaluation of Remote Sensing Systems, CASC, 500,000¥	*2024 - 2024*
[PI] Computational Storage Based Big Data Processing, MIP, 1,300,000¥	*2023 - 2024*
[PI] AI-Assisted Domain Specific Architecture Design, SKLP, 300,000¥	*2023 - 2024*
[PI] Resilient AI Tool Chain for COTS Devices, CASC, 300,0000¥	*2023 - 2023*
[PI] Elastic Fault-tolerant DLA Architecture, NSFC, 570,000¥	*2022 - 2025*
[PI] Energy-efficient Graph Processing Acceleration on FPGAs, NSFC, 270,000¥	*2020 - 2022*
[PI] Automatic DLA Hardening, SKLCA, 300,000¥	*2021 - 2022*
[Co-PI] Cross-Layer Chip DSE Methods, NKRDP, 1,600,0000¥	*2023 - 2025*
[Co-PI] Micostorage-based Computational Storage, Huawei, 1,200,000¥	*2023 - 2024*
[Co-PI] Open AIoT Processor Architecture Design, CAS, 12,000,000¥	*2020 - 2021*
[Co-PI] Computation Storage based Stream Processing, Huawei, 1,200,000¥	*2020 - 2021*

PUBLICATIONS

[1] X. Zhang, **C. Liu**, S. Liang, C. Xiong, Y. Zhang, H. Li, and X. Li, "Frontier-guided Graph Reordering," *The 30th ACM SIGPLAN Annual Symposium on Principles and Practice of Parallel Programming (PPoPP)*, 2025 (poster).

[2] G. Li, C. Chen, S. Ye, Y. Wang, F. Yang, T. Cao, M. M. S. Aly, **C. Liu**, and M. Yang, "Lut-dla: Lookup table as efficient extreme low-bit deep learning accelerator," *The 31st IEEE International Symposium on High-Performance Computer Architecture(HPCA)*, 2025.

[3] Z. Yuan, L. Dai, W. Li, J. Zhang, Y. Wang, **C. Liu**, H. Li, X. Li, J. Guo, P. Wang, R. Chen, and G. Zhang, "Neuvsa: A unified and efficient accelerator for neural vector search," *The 31st IEEE International Symposium on High-Performance Computer Architecture(HPCA)*, 2025.

[4] X. Zhang, C. Liu, S. Liang, H. K.-h. So, Y. Wang, L. Zhang, H. Li, and X. Li, "TaijiGraph: An Out-of-core Graph Processing System Enhanced with Computational Storage," *The 39th IEEE International Parallel & Distributed Processing Symposium (IPDPS)*, 2025.

[5] M. Chen, **C. Liu**, S. Liang, L. He, Y. Wang, L. Zhang, H. Li, and X. Li, "An energy-efficient in-memory accelerator for graph construction and updating," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 2024.

[6] M. Chen, T. Han, **C. Liu**, S. Liang, K. Yu, L. Dai, Z. Yuan, Y. Wang, L. Zhang, H. Li, and X. Li, "DRIM-ANN: An Approximate Nearest Neighbor Search Engine based on Commercial DRAM-PIMs," *arXiv preprint arXiv:2410.15621*, 2024.

[7] L. Cheng, Y. Gu, Q. Liu, L. Yang, **C. Liu**, and Y. Wang, "Advancements in accelerating deep neural network inference on aiot devices: A survey," *IEEE Transactions on Sustainable Computing*, 2024.

[8] L. Dai, Z. Yuan, S. Liang, W. Li, K. Zou, Y. Wang, **C. Liu**, H. Li, and X. Li, "Agc: A unified architecture for accelerating k-nearest neighbor graph construction in vector search," in *2024 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, 2024, pp. 1–9.

[9] F. Fu, W. Zhang, Z. Jiang, Z. Zhu, G. Li, B. Yang, **C. Liu**, L. Xiao, J. Wang, H. Li, and X. Li, "Sigdla: A deep learning accelerator extension for signal processing," *arXiv preprint arXiv:2407.12565*, 2024.

[10] J. Gong, **C. Liu**, L. Cheng, H. Li, and X. Li, "Mcu-mixq: A hw/sw co-optimized mixed-precision neural network design framework for mcus," *arXiv preprint arXiv:2407.18267*, 2024.

[11] H. Huang, **C. Liu**, B. Liu, H. Li, and X. Li, "MRFI: An Open Source Multi-Resolution Fault Injection Framework for Neural Network Processing," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 2024.

[12] Y. Hui, Q. Li, L. Wang, **C. Liu**, D. Zhang, and X. Miao, "In-memory wallace tree multipliers based on majority gates within voltage-gated sot-mram crossbar arrays," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 2024.

[13] Z. Jiang, Q. Zhang, **C. Liu**, H. Li, and X. Li, "Iicpilot: An intelligent integrated circuit backend design framework using open eda," *arXiv preprint arXiv:2407.12576*, 2024.

[14] Z. Wang, T. Luo, **C. Liu**, W. Liu, R. S. M. Goh, and W.-F. Wong, "Enabling energy-efficient deployment of large language models on memristor crossbar: A synergy of large and small," *IEEE Transactions on Pattern Analysis and Machine Intelligence (TPAMI)*, 2024.

[15] C. Xiong, **C. Liu**, H. Li, and X. Li, "Hlspilot: Llm-based high-level synthesis," in *2024 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, 2024, pp. 1–9.

[16] X. Xue and **C. Liu**, "Adaptive soft error protection for deep learning," *arXiv preprint arXiv:2407.19664*, 2024.

[17] Q. Zhang, **C. Liu**, S. Liu, Y. Hui, H. Li, and X. Li, "Approxpilot: A gnn-based accelerator approximation framework," *arXiv preprint arXiv:2407.11324*, 2024.

[18] X. Zhang, Z. Feng, S. Liang, X. Chen, **C. Liu**, H. Li, and X. Li, "Graphitron: A domain specific language for fpga-based graph processing accelerator generation," *arXiv preprint arXiv:2407.12575*, 2024.

[19] P.-o. S. Book, "Built-in fault-tolerant computing paradigm for resilient large-scale chip design a self-test, self-diagnosis, and self-repair-based approach," 2023.

[20] L. Cheng, Y. Wang, F. Cheng, **C. Liu**, Z. Zhao, and Y. Wang, "A deep reinforcement learning-based preemptive approach for cost-aware cloud job scheduling," *IEEE Transactions on Sustainable Computing*, 2023.

[21] C. Chu, **C. Liu**, D. Xu, Y. Wang, T. Luo, H. Li, and X. Li, "Accelerating deformable convolution networks with dynamic and irregular memory accesses," *ACM Transactions on Design Automation of Electronic Systems*, vol. 28, no. 4, pp. 1–23, 2023.

[22] C. Gao, Y. Wang, **C. Liu**, M. Wang, W. Chen, Y. Han, and L. Zhang, "Layer-puzzle: Allocating and scheduling multi-task on multi-core npus by using layer heterogeneity," in *2023 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, IEEE, 2023, pp. 1–6.

[23] Y. He, L. Zhang, **C. Liu**, L. Zhang, and Y. Wang, "S {2} loop: A lightweight spectral-spatio loop closure detector for resource-constrained platforms," *IEEE Robotics and Automation Letters*, vol. 8, no. 3, pp. 1826–1833, 2023.

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[25] H. Huang, X. Xue, **C. Liu**, Y. Wang, T. Luo, L. Cheng, H. Li, and X. Li, "Statistical modeling of soft error influence on neural networks," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 2023.

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[28] N. W. Ming, Z. Wang, **C. Liu**, R. S. M. Goh, and T. Luo, "Ma-bert: Towards matrix arithmetic-only bert inference by eliminating complex non-linear functions," in *The 11th International Conference on Learning Representations (ICLR)*, 2023.

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[35] W. Chen, Y. Wang, Y. Xu, C. Gao, **C. Liu**, and L. Zhang, "A framework for neural network architecture and compile co-optimization," *ACM Transactions on Embedded Computing Systems*, vol. 22, no. 1, pp. 1–24, 2022.

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[39] F. Li, Y. Wang, **C. Liu**, H. Li, and X. Li, "Noception: A fast ppa prediction framework for network-on-chips using graph neural network," in *2022 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, IEEE, 2022, pp. 1035–1040.

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[44] X. Zhao, Y. Wang, **C. Liu**, C. Shi, K. Tu, and L. Zhang, "Network pruning for bit-serial accelerators," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 2022.

[45] **C. Liu**, C. Chu, D. Xu, Y. Wang, Q. Wang, H. Li, X. Li, and K.-T. Cheng, "Hyca: A hybrid computing architecture for fault-tolerant deep learning," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 41, no. 10, pp. 3400–3413, 2021.

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[55] M. Wang, Y. Wang, **C. Liu**, and L. Zhang, "Network-on-interposer design for agile neural-network processor chip customization," in *2021 58th ACM/IEEE Design Automation Conference (DAC)*, IEEE, 2021, pp. 49–54.

[56] D. Xu, Z. Feng, **C. Liu**, L. Li, Y. Wang, H. Li, and X. Li, "Taming process variations in cnfet for efficient last-level cache design," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 30, no. 4, pp. 418–431, 2021.

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[58] D. Xu, Z. Zhu, **C. Liu**, Y. Wang, S. Zhao, L. Zhang, H. Liang, H. Li, and K.-T. Cheng, "Reliability evaluation and analysis of fpga-based neural network acceleration system," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 2021.

[59] W. Chen, Y. Wang, S. Yang, **C. Liu**, and L. Zhang, "You only search once: A fast automation framework for single-stage dnn/accelerator co-design," in *2020 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, 2020, pp. 1283–1286.

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